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14EVE21

Second Semester M.Tech. Degree Examination, June/July 2015
Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive the complete small signal model for an NMOS transistor with $I_D = 100\mu A$, $V_{SS} = 1$ V, $V_{DS} = 2$ V, $V_{SB} = 1$V. Device parameters are $\phi_f = 0.3$ V, W = 10 μm, L = 1 μm, $\gamma = 0.5\ V^{1/2}$, $k' = \mu_n C_{ox} = 200\ \mu A/V^2$, $\lambda = 0.02\ V^{-1}$, $t_{ox} = 100$ A°, $\phi_B = 0.6$V, $C_{sbo} = C_{dbo} = 10$ fF. Overlap capacitance to source and gate, drain and gate is 1 fF. Assume $C_{gb} = 5$ fF. Assume transistor is in saturation. Also draw the small signal complete model. **(13 Marks)**

b. Describe the variation of gate – source and gain drain capacitance in NMOS transistor with respect to V_{GS} and explain. **(07 Marks)**

2 a. For the circuit shown in Fig. Q2(a), assume the transistor is operating in saturation. For the given circuit find the required V_{BIAS} for which the DC value of the V_{out} is 1.44 V and the small signal gain V_{out}/V_{sig}. Assume : $\lambda = 0$, $\gamma = 1\ V^{1/2}$, $2\phi_F = 0.64$ V, $V_{THO} = 0.4$ V, $\mu_n C_{ox} = 800\ \mu A/V^2$, $\left(\frac{W}{L}\right) = 20$, $R_D = R_S = 0.5\ k\Omega$ and $V_{DD} = 1.8$ V. **(15 Marks)**

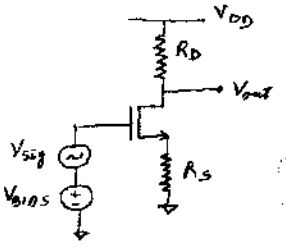

Fig.Q2(a)

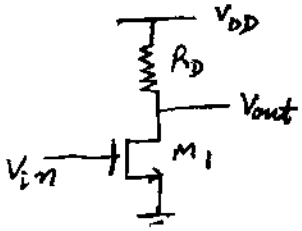

Fig.Q3(b)

b. With help of an example, explain how common drain amplifier can be used as a voltage level shifter. **(05 Marks)**

3 a. Draw the high frequency model of a common source stage along with its equivalent small signal model. For the common source stage drawn derive the transfer function. Assume the gain of the amplifier is constant with reference to frequency and ignore the existence of zero's in the circuit. **(12 Marks)**

b. For the circuit shown in Fig. Q3(b), calculate the total output noise voltage and the input referred noise voltage. **(08 Marks)**

4 a. For the circuit shown in Fig. Q4(a), assume all transistors are in saturation region, $\lambda = 0$ and $\gamma = 0$. For the given circuit find the expression for the small–single differential voltage gain. What will be the new voltage gain if we assume $(W/L)_3 = 0.5\ (W/L)_5$. **(10 Marks)**

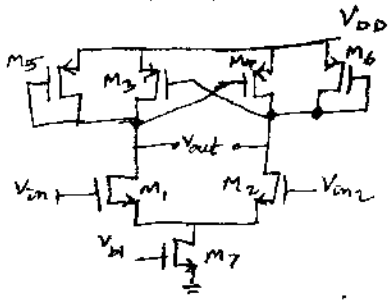

Fig.Q4(a)

b. Draw the basic current mirror circuit. For the current mirror circuit express the output current I_{out} in terms of reference current I_{ref}. What is the effect of channel length modulation on I_{out}? How can the effect of channel length modulation on output current be suppressed? Draw the modified current mirror circuit and explain how the effect of channel length modulation is minimized. **(10 Marks)**

5 Design a two - stage OP-amp based on topology shown in Fig. 5. The design specifications are : V_{DD} = 3V, total power consumption of 3 mW, output swing of 2.6 V, total gain of 1000, L = 0.4 μm for all devices. Use the following assumptions for your Design :

i) Allocate equal overdrive voltage to M_5 and M_6

ii) Assume bias current of the first stage and second stage are equal

iii) $V_{SG3} = V_{SG5}$.

The technology parameters are :

$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3V$, $V_{TH(NMOS)} = V_{TH(PMOS)} = 0.5V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$. **(20 Marks)**

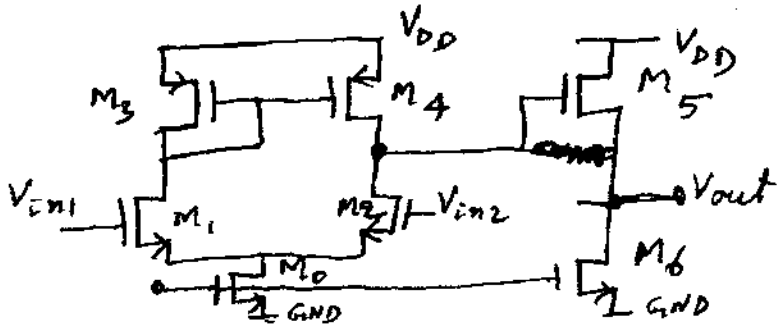

Fig.Q5

6 a. Explain in detail, the various non – ideal effects in PLL. **(10 Marks)**

b. With a neat diagram, explain the working of cross-coupled oscillator. **(10 Marks)**

7 a. Explain the working of reference generator incorporating two series base – emitter voltages shown in Fig. 7(a). **(10 Marks)**

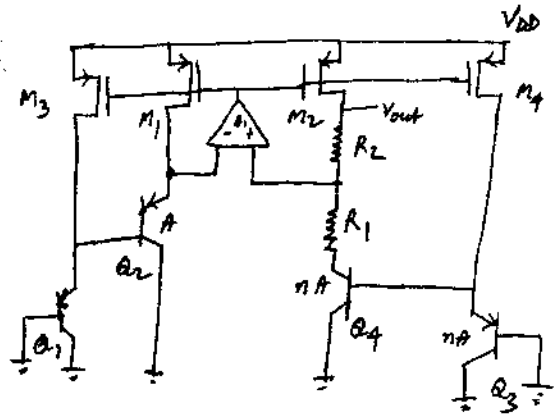

Fig.Q7(a)

b. Explain the three mechanisms in MOS transistor operation which introduce error at the instant MOS transistor switch turns off. **(10 Marks)**

8 a. Explain the working of sample and hold circuit and with a neat diagram explain the typical errors associated with a S/H circuit. **(07 Marks)**

b. Explain the working of a charge scaling DAC. **(08 Marks)**

c. Explain the working of a 3-bit flash ADC. **(05 Marks)**

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